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EXAMINER
RODRIGUEZ, GLENDA P

ART UNIT	PAPER NUMBER
2651	

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/994,009	Applicant(s) HEYDARI ET AL.	
	Examiner Glenda P. Rodriguez	Art Unit 2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Patapoutian et al. (US Patent No. 5, 661, 760).

Regarding Claims 1, 4 and 8, Patapoutian et al. teaches a coded binary sequence, comprising: a first group of consecutive bits, the first group having first and second equally sized portions and representing a first logic level, the bits in the first portion each having a second logic level and the bits in the second portion each having a third logic level (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0") (The description of Patent Application is according to the instant specification, and, it is concurrent with Page 6, Table 1 to Page 7, Line 13 of the instant specification.).); and a second group of consecutive bits, the second group having first and second equally sized portions and representing a fourth logic level, the bits in the first portion each having a fifth logic

level and the bits in the second portion each having a sixth logic level ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claim 2, Patapoutian et al. teaches all the limitations of Claim 1. Patapoutian et al. further teach wherein the first and second equally sized portions of the first group respectively comprise first and second halves of the first group (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that the first group with two equally sized portions (group "10") can be equally divided in to first and second halves: "10" or "--++++--" can be equally divided into "--++" and "++--".); and the first and second equally sized portions of the second group respectively comprise first and second halves of the second group ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claim 6, Patapoutian et al. teaches all the limitations of Claim 1. Patapoutian et al. further teach wherein the first and second groups each respectively comprise four consecutive bits (Patapoulitian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claim 7, Patapoutian et al. teaches all the limitations of Claim 4. Patapoutian et al. further teach the first and second portions of the second group respectively comprises first and second halves of the second group ("11" would be

the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1").).

Regarding Claim 10, Patapoutian et al. teaches a storage disk, comprising: disk sectors operable to store application data (Col. 6, Lines 15-61); and servo wedges that store servo data (Col. 6, Lines 15-61) that includes, a first group of consecutive bits, the first group having first and second equally sized portions and representing a first logic level, the bits in the first portion each having a second logic level and the bits in the second portion each having a third logic level (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0") (The description of Patent Application is according to the instant specification, and, it is concurrent with Page 6, Table 1 to Page 7, Line 13 of the instant specification.).); and a second group of consecutive bits, the second group having first and second equally sized portions and representing a fourth logic level, the bits in the first portion each having a fifth logic level and the bits in the second portion each having a sixth logic level ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claim 11, Patapoutian et al. teaches a Viterbi detector operable to: receive a signal that represents a binary sequence (See Abstract) having a first group of consecutive bits each having a first logic level and a second group of consecutive bits, the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing the first logic level and the second group representing the second logic level (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0").)); and recover the binary sequence from the signal (Col. 11, Lines 3-25 and Lines 57-62. Patapoutian et al. teaches using the Viterbi detector to decode the received data).

Regarding Claim 12, Patapoutian et al. teaches all the limitations of Claim 11. Patapoutian et al. further teaches wherein the binary sequence comprises a coded binary sequence (See Abstract).

Regarding Claim 13, Patapoutian et al. teaches all the limitations of Claim 11. Patapoutian et al. further teach wherein the first logic level comprises a logic 0; and the second logic level comprises a logic 1 (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "10" will be encoded into "--

++++--", having a first and second equally sized portion in the first group ("--++" and "++--").).

Regarding Claim 14, Patapoutian et al. teaches a servo circuit (Col. 6, Lines 38-44), comprising: a sample circuit (See Abstract) operable to generate samples of a signal that represents a coded binary sequence having a first group of consecutive bits each having a first logic level and a second group of consecutive bits, the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing the first logic level and the second group representing the second logic level (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++" (According to the specification it is concurrent with Page 6, Table 1 to Page 7, Line 13.).); and a Viterbi detector (See Abstract) coupled to the sample circuit and operable to recover the coded binary sequence from the samples of the signal (Col. 5, Line 64 to Col. 6, Line 13 and Col. 11, Lines 3-25 and Lines 57-62).

Regarding Claim 15, Patapoutian et al. teaches all the limitations of Claim 14. Patapoutian et al. further teach a decoder coupled to the Viterbi detector and operable to decode the recovered binary sequence (Col. 11, Lines 3-25 and Lines 57-62).

Regarding Claim 16, Patapoutian et al. teaches a disk-drive system, comprising: a data-storage disk having a surface (Col. 5, Lines 15-21), data sectors at respective locations of the surface, and servo wedges that store servo data (Col. 6, Lines 15-61. Servo data are used for non-application purposes.) that includes a first group of consecutive bits each having a first logic level and a second group having first and second portions of consecutive bits, the bits in the first portion having the first logic level and the bits in the third portion having a second logic level, the first group representing the first logic level and the second group representing the second logic level (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++" (According to the specification it is concurrent with Page 6, Table 1 to Page 7, Line 13.).); a motor coupled to and operable to rotate the disk (It is inherent in the art that a disk is rotated by a motor (also referred as spindle motor or driving means)); a read head operable to generate a servo signal that represents the servo data and having a position with respect to the surface of the data-storage disk (Col. 5, Lines 15-21, Lines 28-32 and Lines 57-63); a read-head positioning circuit operable to move the read head over the surface of the disk (Col. 5, Lines 15-21, Lines 28-32 and Lines 57-63); and a servo circuit coupled to the read head and operable to recover the servo data from the servo signal (Col. 5, Lines 15-21, Lines 28-32 and Lines 57-63).

Regarding Claim 17, Patapoutian et al. teaches all the limitations of Claim 16. Patapoutian et al. further teaches wherein the servo circuit comprises: a sample circuit operable to generate samples of the servo signal (See Abstract); and a Viterbi detector coupled to the sample circuit and operable to recover the servo data from the samples of the servo signal (Col. 5, Line 64 to Col. 6, Line 13 and Abstract and Fig. 1).

Regarding Claim 18, Patapoutian et al. teaches all the limitations of Claim 16. Patapoutian et al. further teaches wherein the servo circuit comprises a decoder operable to decode the recovered servo data (See Abstract. Patapoutian et al. teaches that the Viterbi detector also decodes the ¼ signal.).

Regarding Claim 19, Patapoutian et al. teach all the limitations of Claim 16. Patapoutian et al. further teach wherein the read head comprises a read-write head (Col. 5, Lines 15-21, Lines 28-32 and Lines 57-63 and Col. 12, Lines 1-12).

Regarding Claim 20, Patapoutian et al. teaches a method, comprising: coding a first logic level as a first group of consecutive bits (Col. 7, Lines 27-32), the first group having first and second equally sized portions, the bits in the first portion each having a second logic level and the bits in the second portion each having a third logic level (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level

("1") and a third logic level ("0") (The description of Patent Application is according to the instant specification, and, it is concurrent with Page 6, Table 1 to Page 7, Line 13 of the instant specification.).); and coding a fourth logic level as a second group of consecutive bits, the second group having first and second equally sized portions, the bits in the first portion each having a fifth logic level and the bits in the second portion each having a sixth logic level ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claims 3 and 21, Patapoutian et al. teaches all the limitations of Claims 1 and 20, respectively. Patapoutian et al. further teach wherein the first, second, third, and fifth logic levels equal logic 0; and the fourth and sixth logic levels equal logic 1 (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that these logic levels can be achieved according to the configuration of zeros and ones that the disk drive enhances.).

Regarding Claim 22, Patapoutian et al. teaches al the limitations of Claim 20. Patapoutian et al. further teaches wherein the coding comprises: coding the first logic level as a first group of four consecutive bits (Patapoulitian et al. teaches that each group of bits consists of 4 consecutive bits (Col. 3, Lines 55-58. Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--"); and coding the fourth logic level as a second group of four consecutive bits (Patapoulitian et al. teaches that each group of bits consists of 4

consecutive bits (Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claim 23, Patapoutian et al. teaches all the limitations of Claim 20. Patapoutian et al. further teach wherein the first and second portions of the first group and the first and second portions of the second group respectively comprise first and second halves of the first and second groups ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claim 24, Patapoutian et al. teaches a method, comprising: coding a first bit of servo data as a first group of four consecutive bits each having a first logic level; and coding a second bit of servo data as a second group of four consecutive bits respectively having the first logic level, the first logic level, a second logic level, and the second logic level (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0") (According to the specification it is concurrent with Page 6, Table 1 to Page 7, Line 13.).).

Regarding Claim 27, Patapoutian et al. teaches a method, comprising: writing a first code symbol into a servo wedge of a data-storage disk (Col. 6, Lines 15-61. Servo data are used for non-application purposes.), the first code symbol having a

length and representing a first logic level (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0") (According to the specification it is concurrent with Page 6, Table 1 to Page 7, Line 13.).); and writing a second code symbol (Col. 1, Lines 46-52) into the servo wedge, the second code symbol having the length or approximately the length, a first portion, and a second portion, and representing a second logic level, the first portion having a different value than the second portion ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claim 28, Patapoulitian et al. teaches all the limitations of Claim 27. Patapoulitian et al. further teaches wherein: the first and second code symbols each comprise a number of code bits (Patapoulitian et al. teaches that each group of bits consists of 4 consecutive bits (Col. 3, Lines 55-58). Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").); and the lengths of the first and second code symbols are each less than the product of the number and a length of a servo-bit region (Patapoulitian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claims 25, 26 and 29, Patapoutian et al. teaches all the limitations of Claims 24 and 27, respectively. Patapoutian et al. further teach wherein: the first bit equals a logic 0; and the second bit equals a logic 1 (Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that these logic levels can be achieved according to the configuration of zeros and ones that the disk drive enhances.).

Regarding Claim 30, Patapoutian et al. teaches all the limitations of Claim 27. Patapoutian et al. further teaches wherein the first and second portions of the second code symbol are or are approximately half as long as the second code word ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1").).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Aziz (US Patent No. 6, 606, 728), wherein it teaches a (M/N) code encoder, detector and decoder for controlling data which also teach a ¼ biphase coding scheme for controlling servo data (Col. 14, Table 2, and Col. 8, Lines 7-20).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (703) 305-8411. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (703) 308-4825. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9000.

gpr
October 22, 2003.

DAVID HUDSPETH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600